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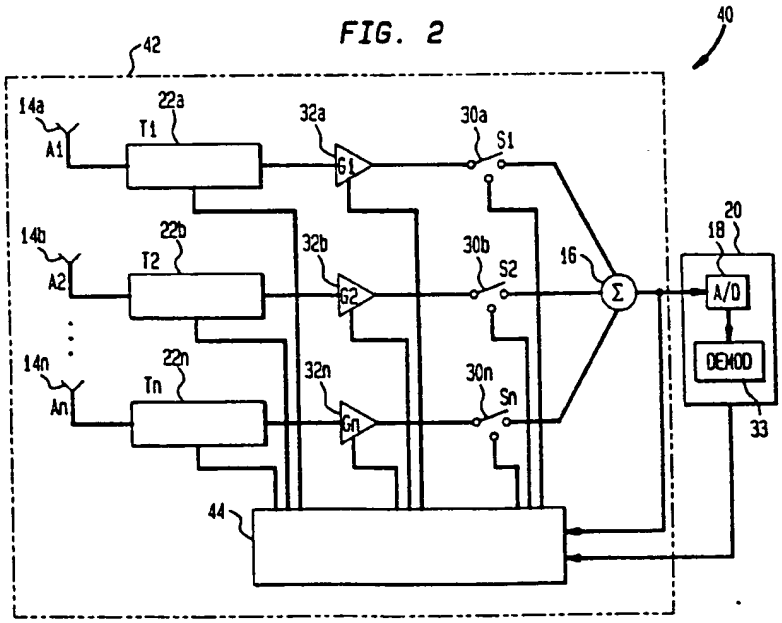
(54) Delay line antenna array system

(57) An antenna array system combines the antenna signals from separate antennas (14a,14b) using at least one delay (22) in the RF path of an antenna. In certain embodiments, the antenna array system combines (at 16) the antenna signals in the Radio Frequency (RF) domain before analog-to-digital (A/D) conversion (18), thereby reducing the amount of hardware required when compared to antenna array systems where the antenna signals are combined digitally. The antenna array system may select parameter settings for the antenna array to provide enhanced performance.

FIG. 2



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to antenna arrays in general and, more particularly, to a delay line antenna array system.

2. Description of the Related Art

Antenna arrays have advantages over single, omnidirectional antennas due to three general characterisitics of antenna arrays. First, antenna arrays provide a signal-to-noise ratio (SNR) gain equal to the number of antennas. Second, antenna arrays can reduce multipath delay spread and fading fluctuations of the received signal because the antenna array can focus on the reception of one or more strong path signals with low relative delays while signals with large excess delays can be attenuated. Third, antenna arrays can separate signals from different users transmitting at the same frequency. These three characteristics for antenna arrays enhance the capacity of wireless, indoor and outdoor networks.

A disadvantage associated with antenna arrays is complexity. Multiple receivers are needed, one for each antenna, and existing methods of combining the different antenna signals are rather complicated and costly. For example, if the different antenna signals are combined digitally, analog-to digital converters are required for the different antennas. Accordingly, an antenna array system is needed which provides the advantages associated with antenna arrays while reducing the complexity and costs of current antenna array systems.

SUMMARY OF THE INVENTION

The present invention relates to an antenna array system which combines the antenna signals from separate antennas using at least one delay in the RF path of an antenna. In certain embodiments, the antenna array system combines the antenna signals in the Radio Frequency (RF) domain before analog-to-digital (A/D) conversion, thereby reducing the amount of hardware required when compared to antenna array systems where the antenna signals are combined digitally. In accordance with other aspects of the present invention, the antenna array system selects delay settings for the antenna array to provide enhanced performance.

BRIEF DESCRIPTION OF THE DRAWING

Other aspects and advantages of the present invention may become apparent upon reading the following detailed description and upon reference to the drawings in which:

FIG. 1 depicts a general block diagram of a receiver using an embodiment of the antenna array system according to the principles of the present invention;
FIG. 2 depicts in block diagram form another embodiment of the antenna array system according to the principles of the present invention;
FIG. 3 depicts a flow chart showing an embodiment of the operation of the antenna array system according to certain principles of the present invention; and
FIG. 4 shows a particular embodiment of a variable delay as a cascade of switchable delay lines according to other principles of the present invention.

DETAILED DESCRIPTION

Illustrative embodiments of the antenna array system according to the principles of the present invention are described below as the antenna array system might be implemented to reduce costs and enhance performance of a wireless receiver.

FIG. 1 shows a simple block diagram of a receiver 10 using a simple embodiment of the antenna array system 12 according to the principles of the present invention.

The antenna array system 12 includes separate antennas 14a and 14b which have spatial separation and/or different polarisations. A combiner 16 combines the signals from the separate antennas 14a and b. In certain embodiments, the antenna signals are physically combined in the RF domain before analog-to-digital (A/D) conversion by an A/D converter 18 in the remainder 20 of the receiver 10. The antenna 14b is connected to a delay 22. The delay 22 can be

set to a delay invoking a lagging phase rotation of the center frequency of the channel to be received. For example, in this particular embodiment, the delay 22 can be set to lagging phase rotations of 0, 90, 180 or 270 degrees. Alternatively, the delay 22 can be set to other phase rotations, and the differences between the phase rotations are not necessarily equal. Additionally, in this particular embodiment, a single delay 22 is shown in the path of the antenna 14b, but an additional delay is possible in the path of the antenna 14a.

The antenna array system 12 includes processing circuitry 24 which can include a microprocessor (not shown) running software, memory (not shown) and/or detection circuitry (not shown) according to aspects of the present invention. The processing circuitry 24 can alternatively be a portion of receiver control circuitry and/or a digital signal processor (DSP). Additionally, the processing circuitry can include an application specific integratec circuit(s) and/or various discrete components.

In this particular embodiment, the processing circuitry 24 sets a delay line 22 to rotate the center frequency of the channel to be received to zero (0) degrees. Upon reception of a transmitted signal in the receive channel, the processing circuitry 24 of this particular embodiment obtains signal quality information for the transmitted signal in the receive channel at 0 degrees and retains the result. In this particular embodiment, the processing circuitry 24 stores the result in a memory location 1. In this particular embodiment, the signal processing information is provided over line 31 from a demodulator 33 using a DSP. Depending on the application, the processing circuitry 24 can measure and determine signal quality information from the transmitted signal. The processing circuitry 24 can also receive and use signal quality information from the demodulator 33 without requiring additional calculation, or the processing circuitry 24 can receive signal quality information measured by other components and perform additional calculations and manipulation of the signal quality information to obtain the desired signal quality information. Signal quality information can include a power estimate from the Automatic Gain Control (not shown) and/or the Mean Square Error from the equalizer (not shown). Alternatively, line 32 can provide received voltage which in some applications can give sufficient information.

The processing circuitry 24 then sets the delay line 22 to rotate the center frequency of the channel to be received to -90 degrees. Upon receiving the transmitted signal in the receive channel, the processing circuitry 24 obtains the signal quality and stores the result in a memory location 2. Next, the processing circuitry 24 sets the delay line 22 to rotate the center frequency of the channel to be received to -180 degrees. Upon receiving the transmitted signal in the receive channel, the processing circuitry 24 obtains the signal quality of the received signal and stores the result in memory location 3. Finally, in this particular embodiment, the processing circuitry 24 sets the delay line 22 to rotate the center frequency of the channel to be received to -270 degrees. Upon receiving the transmitted signal in the receive channel, the processing circuitry 24 obtains the signal quality and stores the result in a memory location 4. In this particular embodiment, the processing circuitry 24 examines the contents of the above memory locations 1-4 and selects which delay line setting resulted in the desired signal quality with respect to the applied quality measure. The processing circuitry 24 sets the delay line 22 to the corresponding setting and proceeds in processing the remainder of the received signal in the channel to be received. Alternatively, the desired signal quality for an antenna path can be determined by using a variable storing the most desirable signal quality value and a variable storing the corresponding delay value for the path and replacing those values when a more desirable signal quality measurement for the antenna path is made.

FIG. 1 shows the signal path for the antenna 14b comprising the delay line 22 and a switch 30. The signal path for the antenna 14b is shown in FIG. 1 directly connected to the combiner 16. In certain embodiments, the processing circuitry 24 can disconnect the signal path for the antenna 14b using the switch 30. After which, the processing circuitry 24 determines the signal quality of the transmitted signal through the signal path of the antenna 14a only and stores the result in an extra memory location 5. As such, the processing circuitry 24 can examine the signal quality of the transmitted signal with only the antenna 14a in addition to the signal quality measurements for the various delay settings in the signal path of the antenna 14b. If the signal quality of the transmitted signal with only the antenna 14a is desired, the processing circuitry 24 can proceed in processing the remainder of the received signal with only the antenna 14a.

FIG. 2 shows a block diagram of an embodiment of a receiver 40 which uses more than two (2) antennas according to the principles of the present invention. This particular embodiment has n circuit paths where path i is the ith path for i = 1...n Each path i has an antenna 14i (A_i), a delay line 22i (D_i), a switch 30i (S_i) and optionally a low noise amplifier 32i (G_i). The low noise amplifier 32i can be configured to replace the switch Si to turn the path i off and on. The delay line 22i, the switch 30i and the amplifier 32i can be cascaded in a different sequence. The outputs of all the paths i are summed by the combiner 16 and fed to the remainder 20 of the receiver 40. In this embodiment, the remainder 20 of the receiver 40 includes an analog-to-digital conversion of the output from the combiner 16.

In this particular embodiment, the switch 30a of the first path is always on, so the switch 30a can be removed. The delay line 22a (D_1) in this particular embodiment only provides a reference rotation D_1=0. Alternatively, different delay values or settings for the delay line 22a can be examined, and the path 1 of the antenna 14a can operate in the same manner as other paths i with minor changes in the described scheme. In this particular embodiment, each of the other delay lines 22b-n (D_2-D_n) are capable of decrementing the phase of the center frequency of the band in m discrete steps as controlled by processing circuitry 44. For each of the delay lines 22b-n (D_2-D_n), the processing circuitry 44

can decrement the phase of the center frequency from 0 to almost 360 degrees, i.e., d_j = [0, (1*360)/m, (2*360)/m, ... ((m-1)*360)/m]. Although in this particular embodiment the decrements are equal, the phase decrements or shifts are not necessarily equal.

The processing circuitry 44 adjusts the delay values for the delays 22a-n for enhanced reception in an effective, efficient and simple manner according to the principles of the present invention. Initially, reception of the transmitted signal occurs using only the antenna 14a (path 1), and the processing circuitry 44 receives and/or determines the signal quality value for the transmitted signal and retains the signal quality value, for example, by storing the signal quality value in memory as a variable. Next, the processing circuitry 44 switches on the second antenna 14b (path 2) by sending a signal to the switch 30b (S_2). The path 2 starts with a phase zero delay (d_1), and in this particular embodiment, the processing circuitry 44 stores the signal quality for the received signal in another memory location for comparison with the other delay values d_2 ..d_m in determining the best signal quality value for the path 2. The processing circuitry 44 then changes the delay value d_j of the delay 22b in decremental steps and at each step in this particular embodiment, the processing circuitry 44 determines the signal quality for the received signal and compares the current signal quality value for the path 2 with the previous best signal quality value for the path 2. The processing circuitry 44 determines the best signal quality measure and corresponding delay for the path 2 and sets the delay 22b to the delay value d_j. Additionally, an overall best signal quality measure variable can be maintained throughout the procedure, and if a path i with any of its delays d_j does not improve the overall best signal quality measure, the processing circuitry 44 can turn off that path i.

After the delay 22b for the path 2 is set, the processing circuitry 44 adds path 3 (if there is a path 3), and the delay 22c is set following the same procedure as described for the path 2. As such, as the paths i are being added, the processing circuitry 44 sets the delays i to the best delay settings or values d_j for each path i in a sequential and cumulative manner. Alternatively, the processing circuitry 44 could determine and retain which paths provided the highest signal quality and set the corresponding delay lines 22i to the best delay settings d_j found after all the paths have been examined.

FIG. 3 shows a flow diagram of a particular embodiment of the operation of the antenna array system 42 (FIG. 2) according to certain principles of the present invention. In this particular embodiment, the processing circuitry 44 retains the best signal quality value and the corresponding best delay j for each path i. As the signal quality for the received signal is determined for each delay value d_j, the processing circuitry 44 sets the delay 22i to the delay value resulting in the best signal quality value for the path i. Initially, the processing circuitry 44 turns off the switches 20b-n (S_2-S_n) at step 50 and sets the delay 22a to an arbitrary delay value, such as zero (0) degrees. The receiver 40 receives the transmitted signal using only the antenna 14a (path 1), and the processing circuitry 44 determines the signal quality of the received signal and stores the signal quality measure as the initial overall best signal quality measure at step 52. Alternatively, the processing circuitry 44 could cycle through decremental delays for the delay 22a of the path 1, determine the signal qualities for the various delay values of the path 1, and maintain the delay value corresponding to the best signal quality measure for the path 1.

The processing circuitry 44 then establishes a loop 54 to cycle through the remaining paths 2 through n, and for each path i, the processing circuitry 44 in this particular embodiment determines the best signal quality for the received signals and the corresponding delay. If the signal quality for the received signal with the current path i and a current delay value d_j is better than the best signal quality measure for the path i, the processing circuitry 44 replaces both the best signal quality measure for the path i with the improved signal quality value and the previous best delay value with the new delay value d_j. As shown, the block 54 starts with i=2, and the processing circuitry 44 adds the second antenna 14b (path 2) at step 56. Step 56 will sequentially add a new path i, and at step 57, the best signal quality for the new path i is initially set at 0 in this particular example. The processing circuitry 44 establishes another loop 58 from 1 to m for j to cycle through the decremental delays d_j for each path i. At step 60, the delay for the path i is set to an initial delay value d_j. At step 61, the processing circuitry 44 measures the signal qualities of the received signals with the path i added having a delay value d_j for the delay 22b.

At step 62, the processing circuitry 44 determines whether the current signal quality measure for the path i is greater than the previous best signal quality measure for the path i. If not, the processing circuitry proceeds to the block 58 to provide another phase delay value d_j for the path i. If so, the processing circuitry 44 proceeds to step 64 to set the best signal quality value D_i for the path i as the current signal quality measure which improves the current best signal quality for the received signal. The processing circuitry 44 sets the best delay value Di for the path i with the delay value corresponding to the best signal quality value for the path i at step 66. After the processing circuitry 44 has measured the signal quality of the received signal for all the delay values d_j for the path i, the processing circuitry 44 determines at step 68 if the best signal quality of the path i has improved the overall best signal quality. If the best signal quality for the path i is greater than the current overall best signal quality, the processing circuitry 44 sets the overall signal quality to the best signal quality at step 70 because the path i with the delay 22i set to delay Di improves the overall signal quality. If the best signal quality for the path i does not improve the overall signal quality, the processing circuitry turns off the path i at step 72.

The processing circuitry then proceeds to block 54 to add the next path i. The next path i is examined in the same manner as the previous path. If all the paths i have been examined, the processing circuitry 44 will receive signals using the paths and the delay settings obtained through this particular embodiment. The processing circuitry 44 can maintain these delay settings until the receiver 40 (FIG. 2) determines that the procedure must be invoked again. Alternative control schemes are possible. For example, the processing circuitry 44 could use all the paths i and use the delay values resulting in the best signal quality values for each path i without turning off any paths i. Alternatively, the processing circuitry 44 can store all the signal quality measurements along with the corresponding stored values of path and delay and perform additional and/or continuous analysis of the signal quality measurements to reset the paths i and corresponding delays 22i. Additionally, the order in which paths i and/or delays d_j for each path i are examined can be changed.

A pseudo-code procedure implementing a particular embodiment of the operation of the antenna array system according to the principles of the present invention can be written as follows:


```
BEGIN
    Turn Switch_i with i = 2...n all off;
    (*to commence only with Path 1*)
    Overall Best Signal Quality = 0;
    Measure Signal Quality and store in memory with corresponding i and j value;
    (*in this case i=1, j=arbitrary*)
    FOR i=2 to n  (*Successively adding Paths by closing Switch_i*)
    DO
    BEGIN
        Add Path_i;
        Best Signal Quality = 0;
        For j=1 to m (*delay line of Path_i is switched stepwise*)
        DO
        BEGIN
            Set delay of path i to j
            Measure Signal Quality and store in memory with corresponding i
            and j values;
            IF Signal Quality > Best Signal Quality
            THEN
            BEGIN
                Best Signal Quality := Signal Quality;
                Best Delay = j; (*The i-th path gets delay setting j*)
            END;
        END;
        Set delay of path i to Best Delay
        if Best Signal Quality > Overall Best Signal Quality,
            Overall Best Signal Quality = Best Signal Quality;
        else    turn off switch i
        END;
END.
```

FIG. 4 shows a particular embodiment of a delay line 22 (FIG. 1, FIG. 2) which can be used in particular embodiments according to the principles of the present invention. The delay line 22i includes (micro)stripline elements 80a and 80b and corresponding switches 82a and 82b. The processing circuitry 44 (FIG. 2) sends control signals over line 84 to control the different switches 82a and b. By controlling the switches 82a and b, the processing circuitry 44 can change the delay value d_j for the variable delay 22i in steps according to the principles of the present invention. For example, the processing circuitry 44 could start examining the various delay values d_j for the path i with the switches 82a and 82 b in the bottom position for the smallest delay. The processing circuitry 44 could change the delay value

d_i for the delay 22i by switching the switches 82a to the top position to introduce the delay value associated with the stripline element 80a. To increase the delay value d_i even further, the processing circuitry 44 could switch the switches 82b to the top position to introduce the delay of the stripline element 80b. In this particular embodiment, only two stripline elements 80a and 80b are shown, but additional stripline elements can be added to increase the amount of delay and/or to increase the resolution between the different delay values for the delay 22i. Additionally, the stripline elements could be different, thereby introducing differing amounts of delay. Finally, the delay d_i for the delay line 22i could be such that the corresponding phase rotation exceeds 360 degrees.

Accordingly, the present invention provides an antenna array system for a wireless receiver that provides enhanced performance with a relatively simple solution. The antenna array system according to the principles of the present invention provides quick and efficient enhancement of signal reception by using an antenna array with at least one antenna path having a delay. The delay value of the delay can be varied, and the delay value resulting in a desirable signal quality as measured by a signal quality measurement(s) is maintained. In accordance with certain aspects of the present invention, the antenna array system provides enhanced performance in a relatively short training time by starting with one antenna (path 1), adding a second antenna (path 2), varying the delay value associated with the second antenna to find a delay configuration which provides the relative best signal quality for the received signal. In certain embodiments, a third antenna (path 3) or more is added in this sequential manner, and the delay values are varied according to the principles of the present invention to find a new delay configuration resulting in a new relatively best signal quality for the received signal.

Certain embodiments of the antenna array system according to the principles of the present invention continue determining delay configurations resulting in better signal quality until all antennas and their associated delays are connected and/or have been examined. Other embodiments can stop determining delay configurations resulting in better signal qualities once a desired signal quality is achieved. Especially in the case of a two antenna array, the delay configuration resulting in enhanced signal reception is realized very quickly which is very important in novice wireless applications in which the training time has to be designed as short as possible. Thus, the antenna array system according to the principles of the present invention provides enhanced receiver performance and the advantages of antenna arrays without the costs or drawbacks associated with current antenna arrays.

Alternative configurations of the antenna array system according to the principles of the present invention are possible which omit or add components, use different schemes, use different delays and/or different delay steps, and/or perform variations of the above-described antenna array system and control thereof. For example, the delay lines 22i (FIG. 2) could be chosen to have particular delay ratios, such as 1:2:4 .... This binary configuration enables n control lines from the processing circuitry 44 (FIG. 2) to set 2^n delays. Other alternative embodiments can be used which are encompassed by the principles of the present invention to provide rapid enhancing of signal reception by using an antenna array of at least two antennas with at least one variable delay and summing the signals from the two paths after the variable delay.

The antenna array system has been described as being comprised several simple components, but it should be understood that the antenna array system and portions thereof can be employed using other forms of delays, switching arrangements, and processing circuitry and variations in the antenna array system and control configuration. For example, the processing circuitry or portions thereof could be employed in existing processing circuitry such as the receiver control processor or digital signal processor. Additionally, the antenna array system according to the principles of the present invention can be implemented utilizing various combinations of application specific integrated circuits, software driven processing circuitry, and/or other arrangements of discrete components. What has been described is merely illustrative of the application of the principles of the present invention. Those skilled in the art will readily recognize that these and various other modifications, arrangements and methods can be made to the present invention without strictly following the exemplary applications illustrated and described herein and without departing from the spirit and scope of the present invention.

Claims

1. An antenna array system, said system CHARACTERIZED BY:

   a first antenna receives communication signals and corresponds to a first path for said communication signals;

   a second antenna receives communication signals and corresponds to a second path for said communication signals, said second path having a delay for said communication signals; and

   a combiner coupled to said first path and said second path, receives said communication signals from said first and second paths and combines said communication signals from said first and second paths.

2. The antenna array system of claim 1 CHARACTERIZED IN THAT said combiner combines said communication

signals from said first and second paths in the Radio Frequency (RF) domain before analog to digital (A/D) con-

INFORMATION DISCLOSURE CITATION FORM FOR PATENT APPLICATION (FORM PTO-1449) Version

Docket No.: 297-01[illegible]-US-PAR) Serial No.: 09/981,101

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Applicant: [illegible]

3. The antenna array system of claim 2 CHARACTERIZED BY a switch connected in said second path which turns said second path off and on.

4. The antenna array system of claim 2 CHARACTERIZED BY a low noise amplifier connected in said second path.

5. The antenna array system of claim 4 CHARACTERIZED IN THAT said low noise amplifier is configured to act as a switch and turn said second path off and on.

U.S. PATENTS

Examiner Initial	Number	Date	Name	Class	Sub-class	Filing date
	5,068,668	11/26/91	Tsuda et al.	342	362	9 e No 11 2[illegible] 95

6. The antenna array system of claim 2 CHARACTERIZED IN THAT said delay is a variable delay and processing circuitry is configured to control said variable delay to change the delay of said variable delay.

7. The antenna array system of claim 2 CHARACTERIZED IN THAT said first path includes a delay.

8. The antenna array system of claim 1 CHARACTERIZED IN THAT said delay is configured as a controllable delay line constructed of a cascade of switchable delay lines to provide variable delays.

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9. An antenna array system, said system CHARACTERIZED BY:

a plurality of antennas receiving communication signals, each antenna corresponds to a separate path for said communication signals;
a delay in at least one of separate paths; and
a combiner coupled to said separate paths, receives said communication signals from said separate paths and combines said communication signals from said separate paths.

10. The antenna array system of claim 9 CHARACTERIZED BY a plurality of said separate paths having delays.

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Sub-class	Translation Yes/No
	EP 0[illegible]	[illegible]	Europe	[illegible]	[illegible]	[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

PATENTTI- JA REKISTERIHALLITUS
Patentti- ja innovaatiolinja

TUTKIMUSRAPORTTI

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FIG. 1

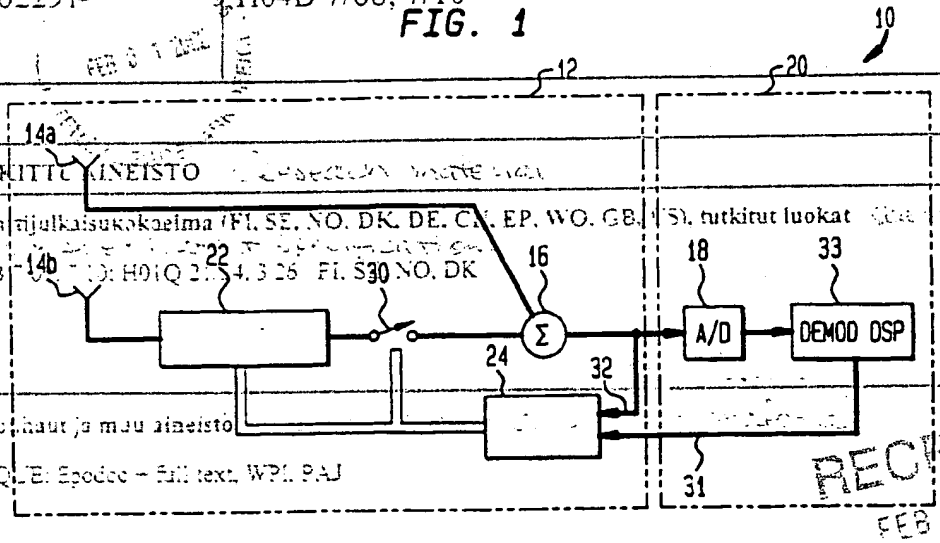

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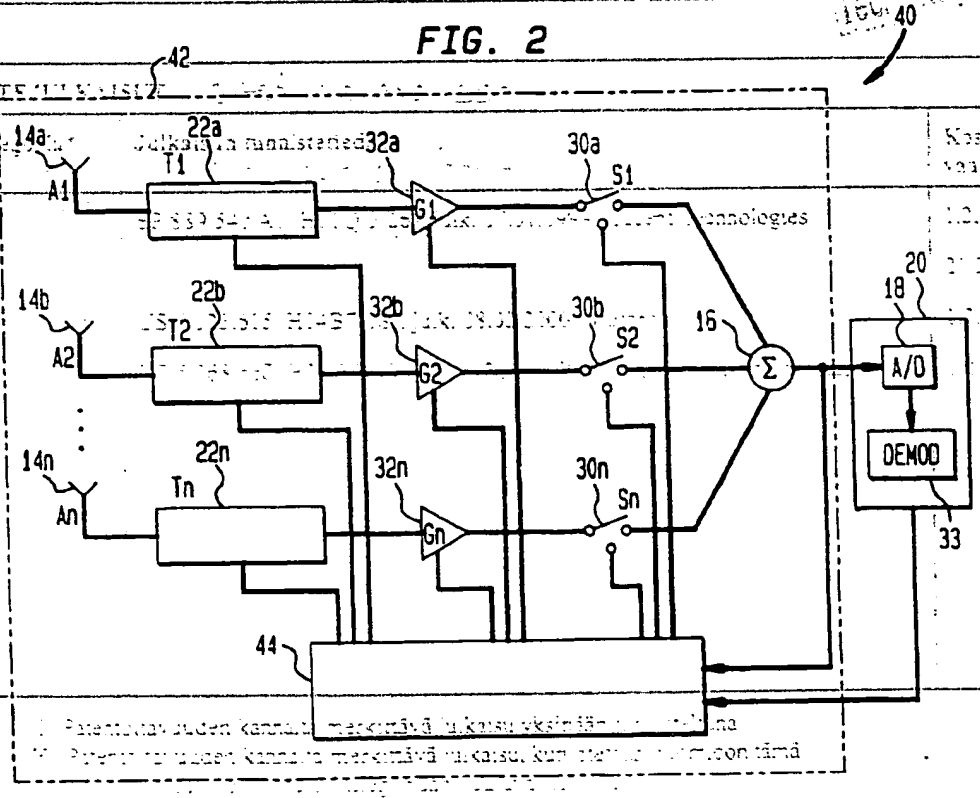
FIG. 2



Päivämäärä Tutkija

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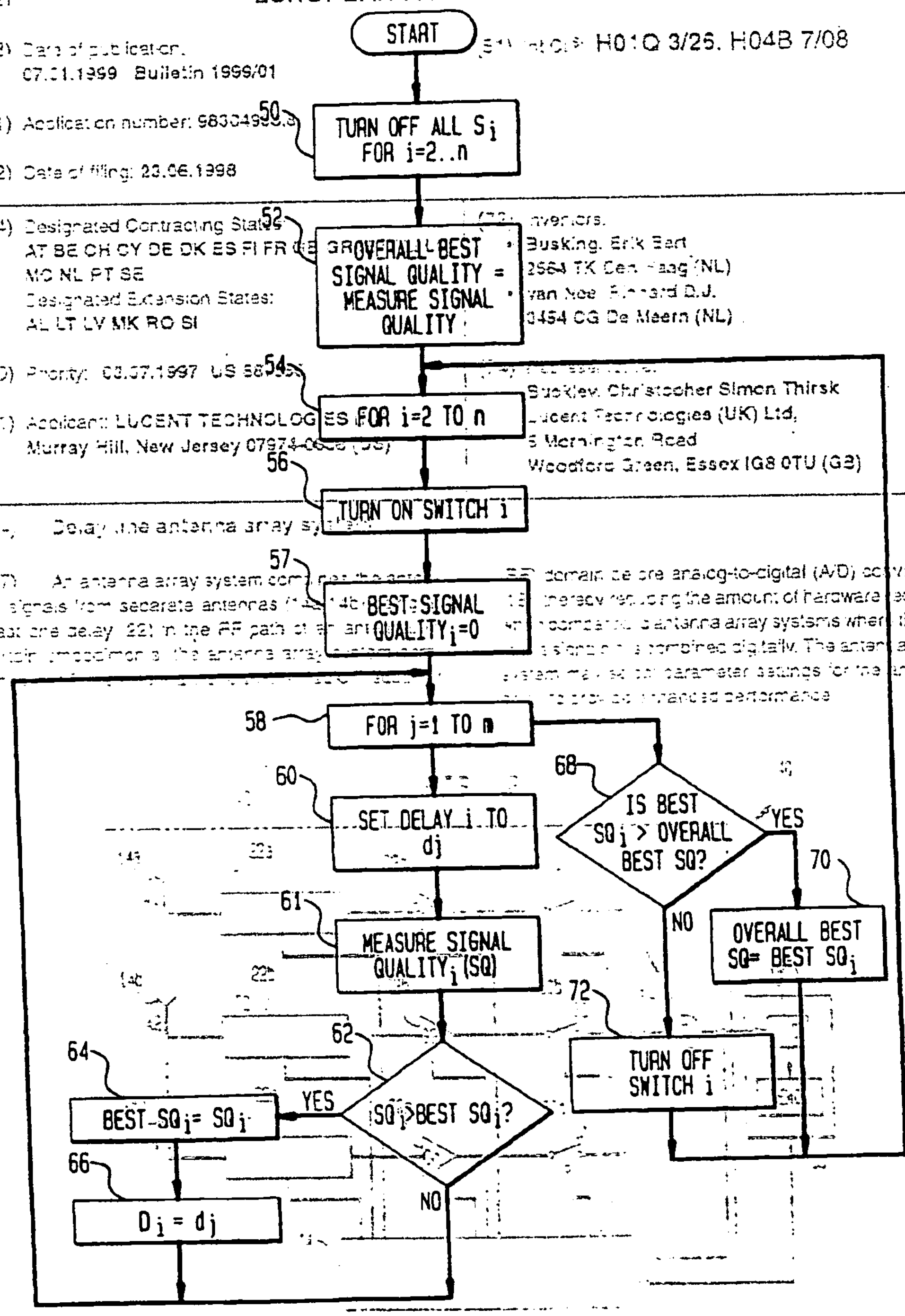
FIG. 3

EUROPEAN PATENT APPLICATION



Description

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to antenna arrays in general and more particularly to a delay line antenna array system.

2. Description of the Related Art

Antenna arrays have advantages over single, omnidirectional antennas due to three general characteristics of antenna arrays. First, antenna arrays provide a signal-to-noise ratio (SNR) gain equal to the number of antennas. Second, antenna arrays can reduce multipath delay spread and fading fluctuations of the received signal because the antenna array can focus on the reception of one or more strong path signals with low relative delays while signals with large excess delays can be attenuated. Third, antenna arrays can separate signals from different users transmitting at the same frequency. These three characteristics for antenna arrays enhance the capacity of wireless, indoor and outdoor networks.

A disadvantage associated with antenna arrays is complexity. Multiple receivers are needed, one for each antenna, and existing methods of combining the different antenna signals are rather complicated and costly. For example, if the different antenna signals are combined digitally, analog-to-digital converters are required for the different antennas. Accordingly, an antenna array system is needed which provides the advantages associated with antenna arrays while reducing the complexity and costs of current antenna array systems.

SUMMARY OF THE INVENTION

The present invention relates to an antenna array system which combines the antenna signals from separate antennas using at least one [illegible] RF path of an antenna. In [illegible] embodiments, the antenna array system combines the antenna signals in the Radio Frequency (RF) domain before analog-to-digital (A/D) conversion, thereby reducing the amount of hardware required when compared to antenna array systems where the antenna signals are combined digitally. In accordance with other aspects of the present invention, the antenna array system selects delay [illegible] to provide [illegible].

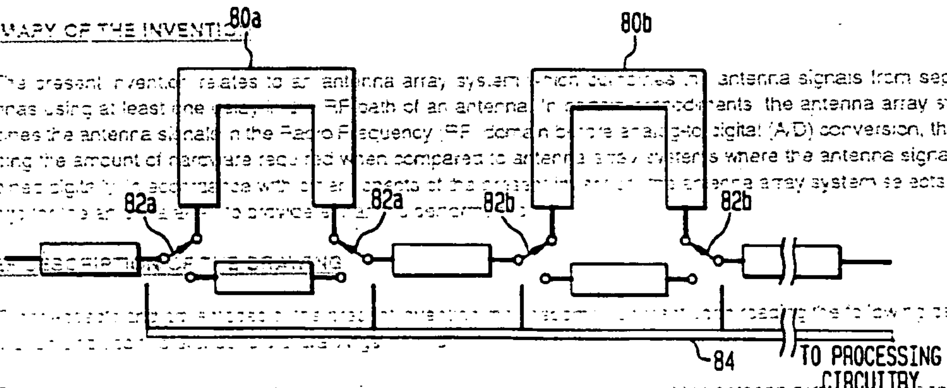


FIG. 4

BRIEF DESCRIPTION OF THE DRAWINGS

[illegible] reading the following detailed description and upon reference to the drawings in which:

FIG. 1 depicts a general block diagram of a receiver using an embodiment of the antenna array system according to the principles of the present invention;

FIG. 2 depicts in block diagram form another embodiment of the antenna array system according to the principles of the present invention;

FIG. 3 depicts a flow chart showing an embodiment of the operation of the antenna array system according to certain principles of the present invention; and

FIG. 4 shows a particular embodiment of a variable delay as a cascade of [illegible] delay lines according to other principles of the present invention.

DETAILED DESCRIPTION

Illustrative embodiments of the antenna array system according to the principles of the present invention are described below as the antenna array system might be implemented to [illegible] costs and enhance performance of a wireless receiver.

FIG. 1 shows a simple block diagram of a receiver 10 using a simple embodiment of the antenna array system 12 according to the principles of the present invention.

[illegible]

set to a delay invoking a lagging phase rotation at the center frequency of the channel to be received. For example, in this particular embodiment the delay 22 can be set to lagging phase rotations of 0, 90, 180 or 270 degrees. Alternatively, the delay 22 can be set to other phase rotations, and the differentials between the phase rotations are not

EUROPEAN SEARCH REPORT

Application Number EP 98 30 4938

DOCUMENTS CONSIDERED TO BE RELEVANT

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 September 1998	Van Dooren, G.

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Application Number
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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 005, no. 063 (E-054), 28 April 1981 & JP 56 013805 A (TOSHIBA CORP;OTHERS: 01), 10 February 1981 * abstract *		
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

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